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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,277	09/16/2003	Hagop A. Nazarian	400.208US01	1468

7590 01/14/2005

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,277	NAZARIAN, HAGOP A.	
	Examiner	Art Unit	
	son t dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

4a) Of the above claim(s) *48-84* is/are withdrawn from consideration.

5)☒ Claim(s) *17-37* is/are allowed.

6)☒ Claim(s) *1-6,15,16,38,39 and 44-47* is/are rejected.

7)☒ Claim(s) *7-14 and 40-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION

The Election filed on 11/24/05 has been entered.

Claims 1-84 are pending in the application.

Claims 48-84 are withdrawn from consideration in view of the election.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 15-16, 38-39, 44-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakui et al (U.S. Patent No 6,049,494).

With respect to claims 1 and 46, Sakui et al disclose a method of operating a non-volatile memory device comprising the steps of :

-coupling a precharge voltage on a substrate tub (by applying Vpre=6V to the channel as shown in figure 14; also see column 17, lines 49-55) on a NAND (the structure of the cell in figure 9 is a NAND structure) architecture memory array of a plurality of floating gate memory cells (as shown in figure 9), wherein the plurality of floating gate memory cells are couple in series (see figure 9),

-coupling a gate programming voltage to the gate of a selected cell of each string (performed by applying Vpgm=18V to the word lines, namely WL2, that is connected to the gate of the floating gate transistor as shown in figure 14),

-selectively coupling a program voltage to a channel of each string of the selected number of strings (this step is preformed by applying Vss to the bit line that connected to the drain of the floating gate transistor. Note that the voltage of the channel of the cell depends on the voltage applied to either the drain or the source of the cell).

With respect of claim 2, the memory device of Sakui et al is clearly an EEPROM (see column 1, lines 8-20).

With respect to claim 3, the programming voltage (the voltage that applied to the word line that directly connects to the gate of the memory cell) is 5-20V (see figure 3B).

With respect to claim 5, the voltage applied to the channel through the drain or the bit line in Sakui is ground (Vss) and the program inhibit (note that the voltage applied to the non-selected cell would be considered as a program inhibit voltage, because this voltage prevent the cell to be programmed) is approximately Vcc (5V or 6V, see figure 14, the voltage applied to bit line).

With respect to claim 6, figure 4 of Sakui et al discloses the step of coupling a pass voltage (the voltage applied to the pass gate or select gate of a non-selected cell) to a non-selected cell.

With respect to claim 15, the circuit for generating voltages to the source and the drain of the cell would be considered as a bit line circuit and source line circuit.

With respect to claim 16, a decoder (column decoder) is inherently included the reference of Sakui et al, since every memory device must have a column decoder connected to a bit line so as to supply a voltage to the bit line in any operation.

With respect to claim 38, the applicant is referred to the rejection applied to claim 1 for the reasons of this rejection. Further, the step of applying a high pass voltage to the gates of the non-selected cell is clearly shown in Sakui et al set forth in the rejection applied to claim 5 above.

With respect to claim 39, the precharge voltage in Sakui et al is applied to the channel that is a part of a substrate tub (see column 18, lines 37-40).

With respect to claims 44 and 45, the Applicant is referred to the rejection applied to claims and 36 for the reasons of this rejection. Also, the voltage applied to the bit line in Sakui et al is transferred to the drain of the cell.

With respect to claim 47, the floating gate transistor in figure 9 of Sakui et al is coupled in series.

Allowable Subject Matter

Claims 17-37 are allowed.

Claims 7-14, 40-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior arts of record fail to teach or disclose a method of operating a memory device comprising the steps of placing a precharge voltage to the substrate and then removing the precharge voltage from the substrate and then applying gate programming voltage to the control gate and a program voltage to the cell so as to program the cell.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Lee teaches a method of operating a memory device including the steps of applying a precharge voltage to a memory cell.

-Choi et al disclose a method of operating a memory device having a step of applying a precharge voltage to a memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-1868.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh

January 12, 2005

Son T. Dinh
Primary Examiner